Title: OPERATION OF A MULTIPLICITY OF TIME SORTED QUEUES …
Inventor Name: Ronald L. Pettyjohn, et al.
Appl. No. Unassigned
Docket No.: CRESC-006XX

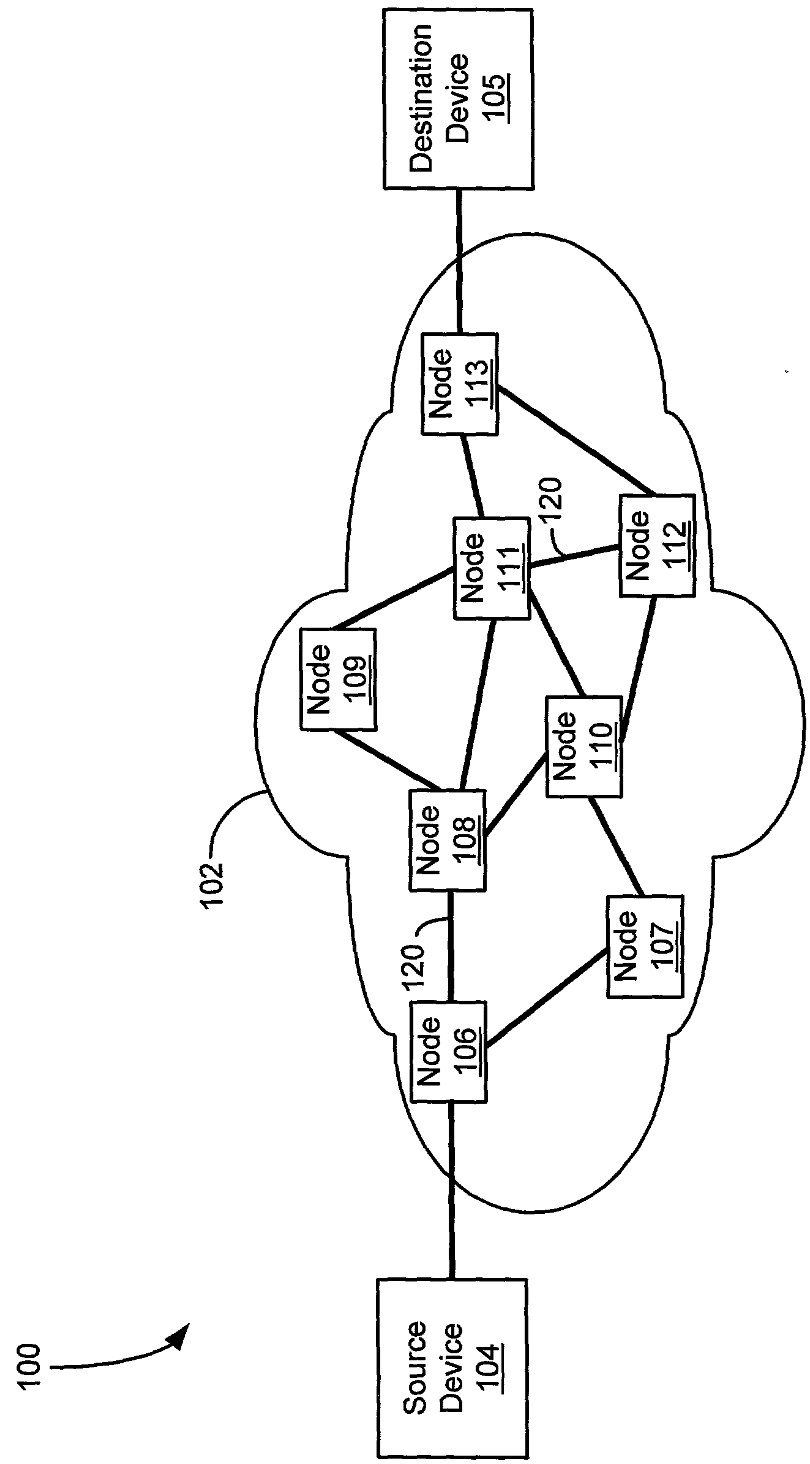

Fig. 1

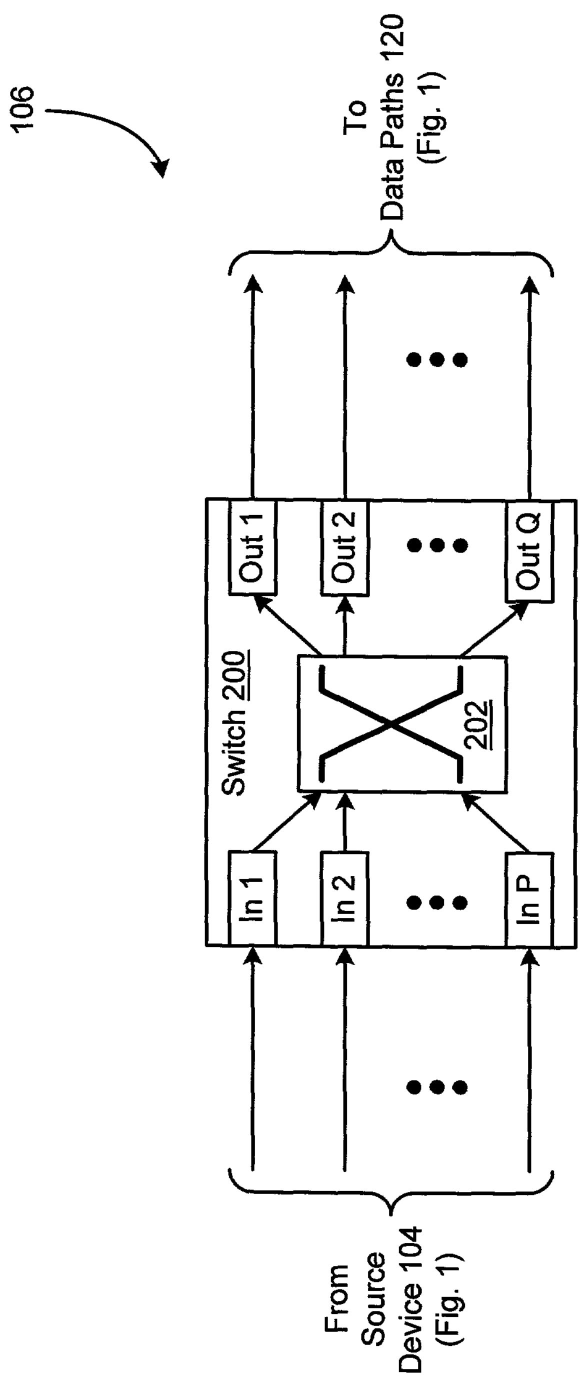
106
To
Data Paths 120
(Fig. 1)
Out 1
Out 2
Out Q
Switch 200
202
In 1
In 2
In P
From
Source
Device 104
(Fig. 1)

Fig. 2

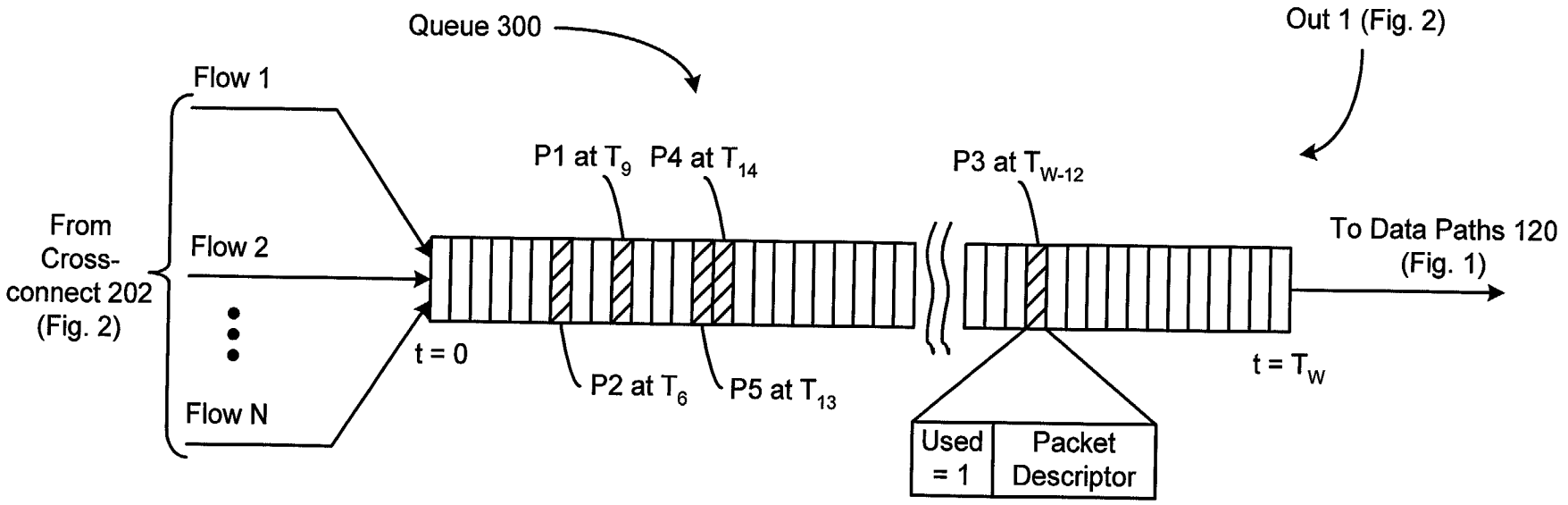

Fig. 3

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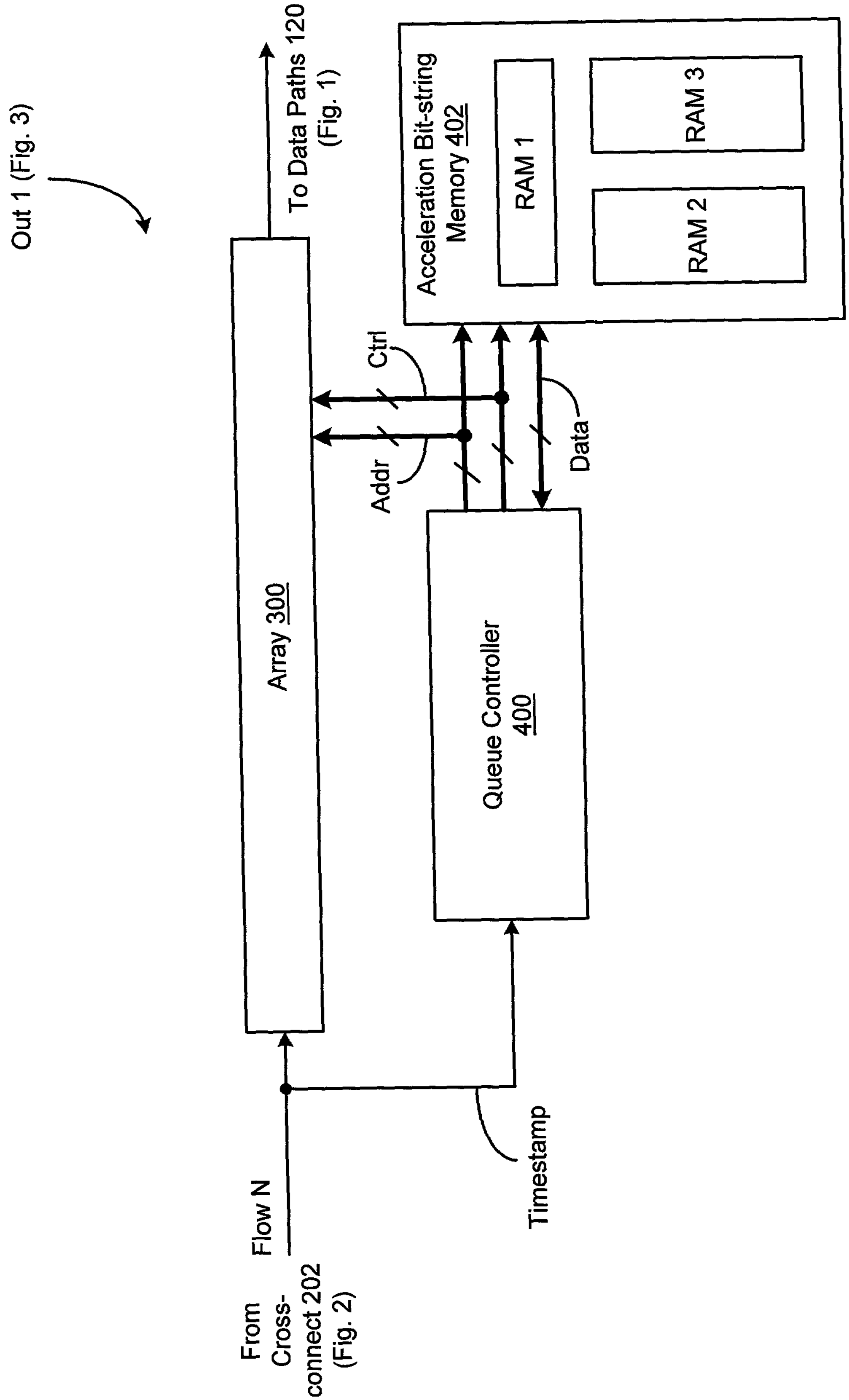
Out 1 (Fig. 3)
To Data Paths 120
(Fig. 1)
Acceleration Bit-string
Memory 402
RAM 1
RAM 2
RAM 3
Ctrl
Addr
Data
Array 300
Queue Controller
400
Flow N
From
Cross-
connect 202
(Fig. 2)
Timestamp

Fig. 4

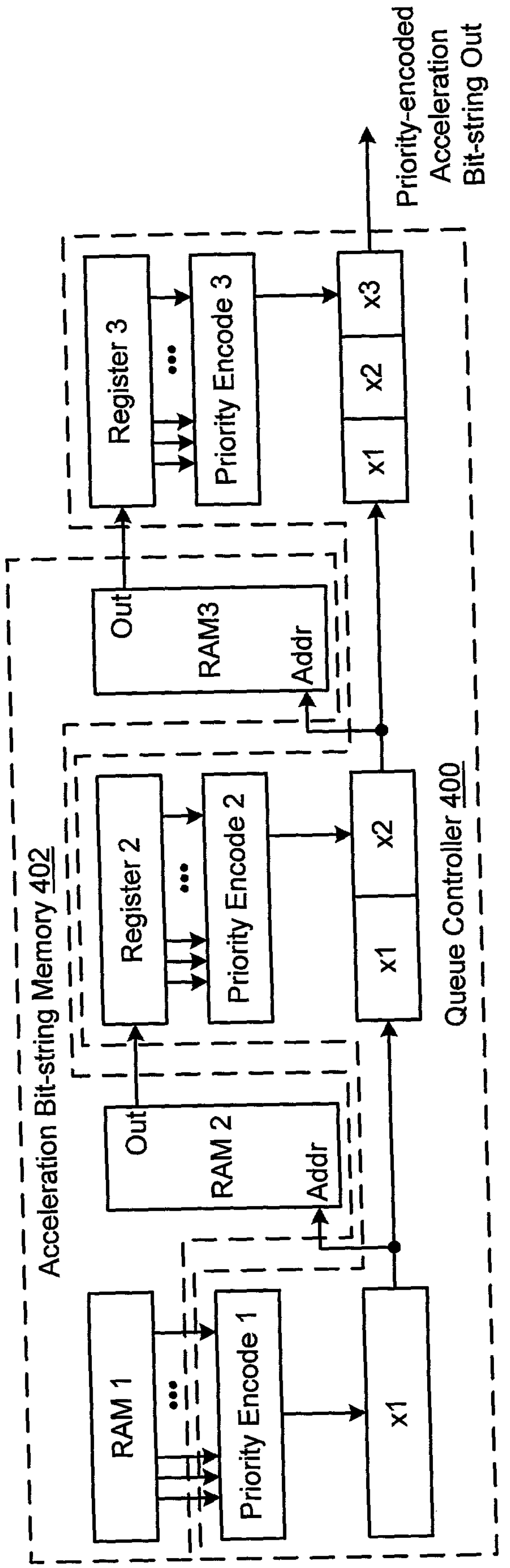
Priority-encoded
Acceleration
Bit-string Out
Register 3
Priority Encode 3
x1
x2
x3
Out
RAM3
Addr
Register 2
Priority Encode 2
x1
x2
Queue Controller 400
Acceleration Bit-string Memory 402
Out
RAM 2
Addr
RAM 1
Priority Encode 1
x1

Fig. 5

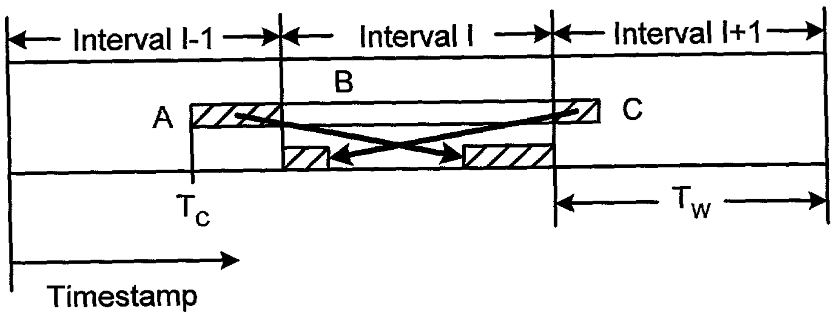

Fig. 6a

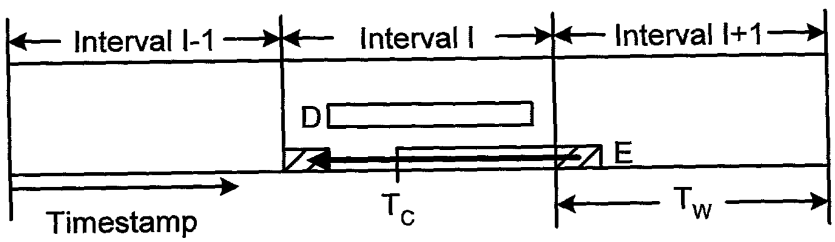

Fig. 6b

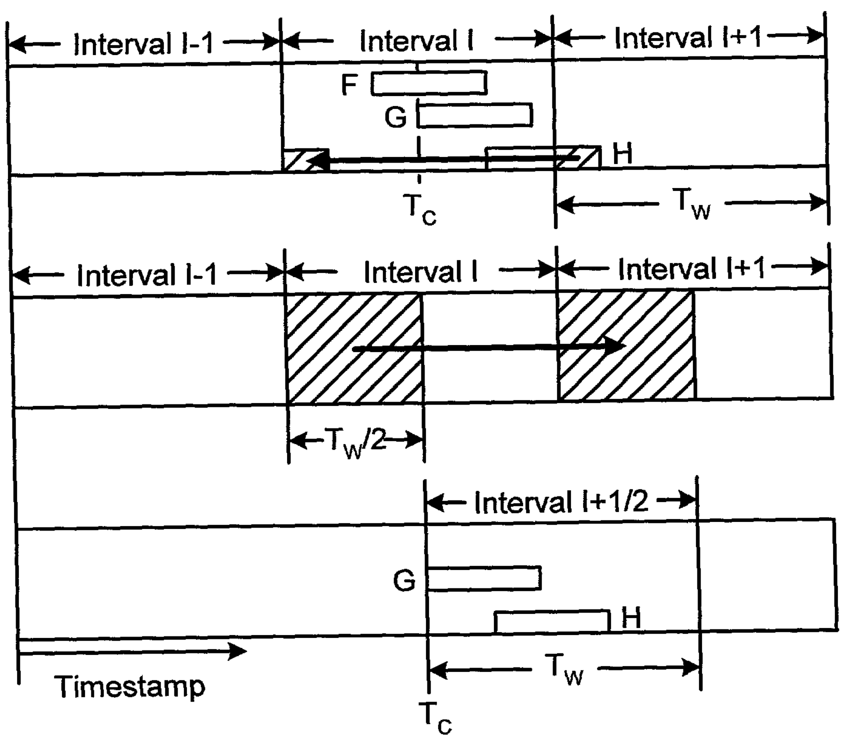

Fig. 6c

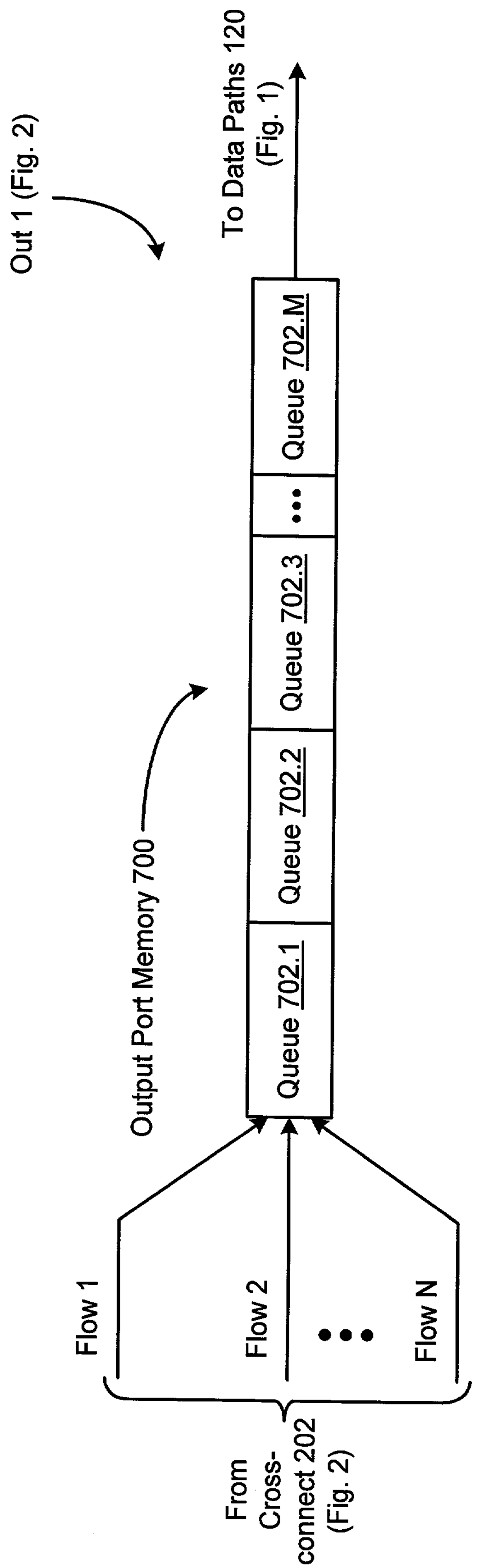
Out 1 (Fig. 2)
To Data Paths 120 (Fig. 1)
Output Port Memory 700
Queue 702.1
Queue 702.2
Queue 702.3
Queue 702.M
Flow 1
Flow 2
Flow N
From Cross-connect 202 (Fig. 2)

Fig. 7

```
//RAM1 = First Level Acceleration Bit-string Memory
//RAM2 = Second Level Acceleration Bit-string Memory
//RAM3 = Third Level Acceleration Bit-string Memory
//ARRAY = Linear Time-Indexed Array
//T = Timestamp Value
//T = T1||T2||T3||TA
// where      T1 = First Timestamp Value Sub-field
//            T2 = Second Timestamp Value Sub-field
//            T3 = Third Timestamp Value Sub-field
//            TA = Fourth Timestamp Value Sub-field
// P = Packet Descriptor
ARRAY[T] <— P     //Timeslot is marked "Used" (Used=1).
RAM1<T1> <— 1
RAM2[T1]<T2> <— 1
RAM3[T1||T2]<T3> <— 1
```

Fig. 8

```
//x1 = First Level Priority-encoded Acceleration
//Bit-string
//x2 = Second Level Priority-encoded Acceleration
//Bit-string
//x3 = Third Level Priority-encoded Acceleration
//Bit-string
x1 <— PRI(RAM1)
x2 <— PRI(RAM2[x1])
x3 <— PRI(RAM3[x1||x2])
X <— x1||x2||x3
//Read N entries of ARRAY starting with ARRAY[X].
P <— ARRAY[K]     //K = the index of the first "Used"
                  //ARRAY entry read.  Timeslot is
                  //marked "Unused" (Used=0).
RAM3[x1||x2]<x3> <— 0   //In the event all ARRAY[X]
                        //through ARRAY[X+N-1] are
                        //now Unused.
RAM2[x1]<x2> <— 0       //In the event RAM3[x1||x2] = 0.
RAM1<x1> <— 0           //In the event RAM2[x1] = 0.
```

Fig. 9